Types of Embedded Processors

- Computational micros (32- or 64-bit datapaths)
 - CPU of workstations, PCs, or high-end portable devices (PDAs)
 - x86, PA-RISC, PowerPC, SPARC, etc.
- Embedded general purpose micros (32-bit datapaths)
 - Designed for a wide range of embedded applications
 - Often scaled-down version of computational micros
 - ARM, PowerPC, MIPS, x86, 68K, etc.
- Microcontrollers (4-, 8-, or 16-bit datapaths)
 - Integrate processing unit, memory, I/O buses, and peripherals
 - Often low-cost, high-volume devices
- Domain-specific processors (datapath size varies greatly)
 - Designed for a particular application domain
 - Digital signal processors, multimedia processors, graphics processors, network processors, security processors, etc.

Embedded Processors For Multimedia And Communications Proceedings Of S P I E

Xiaohua Tian, Thinh M. Le, Yong Lian

Embedded Processors For Multimedia And Communications Proceedings Of S P I E:

High Performance Embedded Architectures and Compilers Yale N. Patt, Pierfrancesco Foglia, Evelyn Duesterwald, Paolo Faraboschi, Xavier Martorell, 2010-01-20 This book constitutes the refereed proceedings of the 5th International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2010 held in Pisa Italy in January 2010 The 23 revised full papers presented together with the abstracts of 2 invited keynote addresses were carefully reviewed and selected from 94 submissions The papers are organized in topical sections on architectural support for concurrency compilation and runtime systems reconfigurable and customized architectures multicore efficiency reliability and power memory organization and optimization and programming and analysis of accelerators Embedded Processors for Multimedia and Communications ,2004 Entropy Coders of the H.264/AVC Standard Xiaohua Tian, Thinh M. Le, Yong Lian, 2010-10-17 This book presents a collection of algorithms and VLSI architectures of entropy or statistical codecs of recent video compression standards with focus on the H 264 AVC standard For any visual data compression scheme there exists a combination of two or all of the following three stages spatial temporal and statistical compression General readers are first introduced with the various algorithms of the statistical coders The VLSI implementations are also reviewed and discussed Readers with limited hardware design background are also introduced with a design methodology starting from performance complexity analyses to software hardware co simulation A typical design of the Contextbased Adaptive Binary Arithmetic Coding CABAC encoder is also presented in details To support System on Chip design environment the CABAC design is wrapped with a SoC based Wishbone system bus interface Embedded Processors for Multimedia and Communications II Subramania I. Sudharsanan, V. Michael Boye (Jr.), Sethuraman Panchanathan, 2005 Proceedings of SPIE present the original research papers presented at SPIE conferences and other high quality conferences in the broad ranging fields of optics and photonics These books provide prompt access to the latest innovations in research and technology in their respective fields Proceedings of SPIE are among the most cited references in patent literature Big Data Benchmarks. Performance Optimization, and Emerging Hardware Jianfeng Zhan, Rui Han, Chuliang Weng, 2014-11-10 This book constitutes the thoroughly revised selected papers of the 4th and 5th workshops on Big Data Benchmarks Performance Optimization and Emerging Hardware BPOE 4 and BPOE 5 held respectively in Salt Lake City in March 2014 and in Hangzhou in September 2014 The 16 papers presented were carefully reviewed and selected from 30 submissions Both workshops focus on architecture and system support for big data systems such as benchmarking workload characterization performance optimization and evaluation emerging hardware High Performance Memory Systems Haldun Hadimioglu, David Kaeli, Jeffrey Kuskin, Ashwini Nanda, Josep Torrellas, 2011-06-27 The State of Memory Technology Over the past decade there has been rapid growth in the speed of micropro cessors CPU speeds are approximately doubling every eighteen months while main memory speed doubles about every ten years The International Tech nology Roadmap for

Semiconductors ITRS study suggests that memory will remain on its current growth path The ITRS short and long term targets indicate continued scaling improvements at about the current rate by 2016 This translates to bit densities increasing at two times every two years until the introduction of 8 gigabit dynamic random access memory DRAM chips after which densities will increase four times every five years A similar growth pattern is forecast for other high density chip areas and high performance logic e q microprocessors and application specific integrated circuits ASICs In the future molecular devices 64 gigabit DRAMs and 28 GHz clock signals are targeted Although densities continue to grow we still do not see significant advances that will improve memory speed These trends have created a problem that has been labeled the Memory Wall or Memory Gap Cryptographic Hardware and Embedded Systems - CHES 2008 Elisabeth Oswald, 2008-07-18 by Andrey Bogdanov Thomas Eisenbarth Andy Rupp and Christopher Wolf The purpose of the award is to formally acknowledge excellence in research We would like to c gratulate the authors of these two papers Multiprocessors Sundararajan Sriram, Shuvra S. Bhattacharyya, 2018-10-03 Techniques for Optimizing Multiprocessor Implementations of Signal Processing Applications An indispensable component of the information age signal processing is embedded in a variety of consumer devices including cell phones and digital television as well as in communication infrastructure such as media servers and cellular base stations Multiple programmable processors along with custom hardware running in parallel are needed to achieve the computation throughput required of such applications Reviews important research in key areas related to the multiprocessor implementation of multimedia systemsEmbedded Multiprocessors Scheduling and Synchronization Second Edition presents architectures and design methodologies for parallel systems in embedded digital signal processing DSP applications It discusses application modeling techniques for multimedia systems the incorporation of interprocessor communication costs into multiprocessor scheduling decisions and a modeling methodology the synchronization graph for multiprocessor system performance analysis The book also applies the synchronization graph model to develop hardware and software optimizations that can significantly reduce the interprocessor communication overhead of a given schedule Chronicles recent activity dealing with single chip multiprocessors and dataflow modelsThis edition updates the background material on existing embedded multiprocessors including single chip multiprocessors It also summarizes the new research on dataflow models for signal processing that has been carried out since the publication of the first edition Harness the power of multiprocessors This book explores the optimization of interprocessor communication and synchronization in embedded multiprocessor systems It shows you how to design multiprocessor computer systems that are streamlined for multimedia applications Hardware/Software Architectures for Low-Power Embedded Multimedia Systems Muhammad Shafique, Jörg Henkel, 2011-07-25 This book presents techniques for energy reduction in adaptive embedded multimedia systems based on dynamically reconfigurable processors The approach described will enable designers to meet performance area constraints while minimizing video

quality degradation under various run time scenarios Emphasis is placed on implementing power energy reduction at various abstraction levels To enable this novel techniques for adaptive energy management at both processor architecture and application architecture levels are presented such that both hardware and software adapt together minimizing overall energy consumption under unpredictable design compile time scenarios Distributed Embedded Systems: Design, Middleware and Resources Bernd Kleinjohann, Lisa Kleinjohann, Marilyn Wolf, 2008-07-10 This year the IFIP Working Conference on Distributed and Parallel Embedded Sys tems DIPES 2008 is held as part of the IFIP World Computer Congress held in Milan on September 7 10 2008 The embedded systems world has a great deal of experience with parallel and distributed computing Many embedded computing systems require the high performance that can be delivered by parallel computing Parallel and distributed computing are often the only ways to deliver adequate real time performance at low power levels This year's conference attracted 30 submissions of which 21 were accepted Prof Jor g Henkel of the University of Karlsruhe graciously contributed a keynote address on embedded computing and reliability We would like to thank all of the program committee members for their diligence Wayne Wolf Bernd Kleinjohann and Lisa Kleinjohann Acknowledgements We would like to thank all people involved in the organization of the IFIP World Computer Congress 2008 especially the IPC Co Chairs Judith Bishop and Ivo De Lotto the Organization Chair Giulio Occhini as well as the Publications Chair John Impagliazzo Further thanks go to the authors for their valuable contributions to DIPES 2008 Last but not least we would like to acknowledge the considerable amount of work and enthusiasm spent by our colleague Claudius Stern in preparing the proceedings of DIPES 2008 Hemade it possible to produce the mintheir current professional and homogeneous style

Dynamic Reconfiguration in Real-Time Systems Weixun Wang, Prabhat Mishra, Sanjay Ranka, 2012-07-20 Given the widespread use of real time multitasking systems there are tremendous optimization opportunities if reconfigurable computing can be effectively incorporated while maintaining performance and other design constraints of typical applications. The focus of this book is to describe the dynamic reconfiguration techniques that can be safely used in real time systems. This book provides comprehensive approaches by considering synergistic effects of computation communication as well as storage together to significantly improve overall performance power energy and temperature. Recent Advances on Video Coding Javier Del Ser Lorente, 2011-07-05. This book is intended to attract the attention of practitioners and researchers from industry and academia interested in challenging paradigms of multimedia video coding with an emphasis on recent technical developments cross disciplinary tools and implementations. Given its instructional purpose the book also overviews recently published video coding standards such as H 264 AVC and SVC from a simulational standpoint Novel rate control schemes and cross disciplinary tools for the optimization of diverse aspects related to video coding are also addressed in detail along with implementation architectures specially tailored for video processing and encoding. The book concludes by exposing new advances in semantic video coding. In summary this book serves as a technically sounding start point for early stage.

researchers and developers willing to join leading edge research on video coding processing and multimedia transmission High-fidelity Multichannel Audio Coding Dai Tracy Yang, Chris Kyriakakis, C.-C. Jay Kuo, 2004 Digital Video Concepts, Methods, and Metrics Shahriar Akramullah, 2014-11-05 Digital Video Concepts Methods and Metrics Quality Compression Performance and Power Trade off Analysis is a concise reference for professionals in a wide range of applications and vocations It focuses on giving the reader mastery over the concepts methods and metrics of digital video coding so that readers have sufficient understanding to choose and tune coding parameters for optimum results that would suit their particular needs for quality compression speed and power The practical aspects are many Uploading video to the Internet is only the beginning of a trend where a consumer controls video quality and speed by trading off various other factors Open source and proprietary applications such as video e mail private party content generation editing and archiving and cloud asset management would give further control to the end user Digital video is frequently compressed and coded for easier storage and transmission This process involves visual quality loss due to typical data compression techniques and requires use of high performance computing systems A careful balance between the amount of compression the visual quality loss and the coding speed is necessary to keep the total system cost down while delivering a good user experience for various video applications At the same time power consumption optimizations are also essential to get the job done on inexpensive consumer platforms Trade offs can be made among these factors and relevant considerations are particularly important in resource constrained low power devices To better understand the trade offs this book discusses a comprehensive set of engineering principles strategies methods and metrics It also exposes readers to approaches on how to differentiate and rank video coding solutions Network and Parallel Computing Erik Altman, Weisong Shi, 2011-10-18 This book constitutes the refereed proceedings of the 8th IFIP International Conference on Network and Parallel Computing NPC 2011 held in Changsha China in October 2011 The 28 papers presented were carefully reviewed selected from 54 submissions The papers are organized in the following topical sections filesystems and data network and parallel algorithms cluster and grid trust and authentication and monitor diagnose and then optimize Multimedia 2001 J.A. Jorge, N.M. Correia, H. Jones, M.B. Kamegai, 2012-12-06 This book presents the results of EG Multimedia 2001 the Sixth Eurographics that Workshop on Multimedia held in Manchester UK on the 8 and 9 of September 2001 All six such workshops are successful examples of fruitful international cooperation under the auspices of the Eurographics working group on Multimedia The workshop covered a wide range of subjects from media production to content processing and delivery with a special focus on issues related to interactive video environments These Dcluded standards and approaches for interactive television hypervideo collaborative video augmented reality mobile multimedia the integration of TV and the Web content analysis processing and presentation The program consisted of two invited keynote presentations eighteen technical papers and one demonstration attracting a diverse world wide group of thirty attendees Technical papers were organized in six sessions spanning the two

days 3D in Multimedia Multimedia Architectures and Authoring ideo and Coding Content Based Retrieval and Security Interactive Media and Interactive TV The demonstration presented a multimedia system for aerobics and fitness training exploring the combination of sound and interactive graphics in an effective manner The keynote presentation by V Michael Bove provided insights into new architectures for large scale pervasive computing The second invited presentation by Glorianna Davenport discussed the relations between creativity and interactive movies as participatory art enabled by new GeoSensor Networks Silvia Nittel, Alexandros Labrinidis, Anthony Stefanidis, 2008-08-15 This volume serves as the post conference proceedings for the Second GeoSensor Networks Conference that was held in Boston Massachusetts in October 2006 The conference addressed issues related to the collection management processing and sis and delivery of real time geospatial data using distributed geosensor networks This represents an evolution of the traditional static and centralized geocomputational paradigm to support the collection of both temporally and spatially high resolution up to date data over a broad geographic area and to use sensor networks as actuators in geographic space Sensors in these environments can be static or mobile and can be used to passively collect information about the environment or eventually to actively influence it The research challenges behind this novel paradigm extend the frontiers of tra tional GIS research further into computer science addressing issues like data stream processing mobile computing location based services temporal spatial queries over geosensor networks adaptable middleware sensor data integration and mining au mated updating of geospatial databases VR modeling and computer vision In order to address these topics the GSN 2006 conference brought together leading experts in these fields and provided a three day forum to present papers and exchange Image Analysis And Recognition Mohamed Kamel, Aurélio Campilho, 2005-09-15 ICIAR 2005 the International ideas Conference on Image Analysis and Recognition was the second ICIAR conference and was held in Toronto Canada ICIAR is organized annually and alternates between Europe and North America ICIAR 2004 was held in Porto Portugal The idea of o ering these conferences came as a result of discussion between researchers in Portugal and Canada to encourage collaboration and exchange mainly between these two countries but also with the open participation of other countries addressing recent advances in theory methodology and applications

TheresponsetothecallforpapersforICIAR2005wasencouraging From295 full papers submitted 153 were nally accepted 80 oral presentations and 73 posters. The review process was carried out by the Program Committee m bersandotherreviewers allareexperts invarious image analysis and recognition areas. Each paper was reviewed by at least two reviewers and also checked by the conference co chairs. The high quality of the papers in these proceedings is attributed rst to the authors and second to the quality of the reviews provided by the experts. We would like to thank the authors for responding to our call andwewholeheartedly thank the reviewers for their excellentwork and for their timely response. It is this collective e ort that resulted in the strong conference program and high quality proceedings in your hands. *Multiprocessor Systems-on-Chips*

Ahmed Jerraya, Wayne Wolf, 2005 Modern system on chip SoC design shows a clear trend toward integration of multiple processor cores on a single chip Designing a multiprocessor system on chip MPSOC requires an understanding of the various design styles and techniques used in the multiprocessor Understanding the application area of the MPSOC is also critical to making proper tradeoffs and design decisions Multiprocessor Systems on Chips covers both design techniques and applications for MPSOCs Design topics include multiprocessor architectures processors operating systems compilers methodologies and synthesis algorithms and application areas covered include telecommunications and multimedia The majority of the chapters were collected from presentations made at the International Workshop on Application Specific Multi Processor SoC held over the past two years The workshop assembled internationally recognized speakers on the range of topics relevant to MPSOCs After having refined their material at the workshop the speakers are now writing chapters and the editors are fashioning them into a unified book by making connections between chapters and developing common terminology Examines several different architectures and the constraints imposed on them Discusses scheduling real time operating systems and compilers Analyzes design trade off and decisions in telecommunications and multimedia applications

Media Processors, 2002

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