Abbreviation Finder

HVL

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Hardware Verification Language

Ehardware Verification Language

L Darling-Hammond

Ehardware Verification Language:

The e Hardware Verification Language Sasan Iman,Sunita Joshi,2007-05-08 I am glad to see this new book on the e language and on verification I am especially glad to see a description of the e Reuse Methodology eRM The main goal of verification is after all finding more bugs quicker using given resources and verification reuse module to system old system to new system etc is a key enabling component This book offers a fresh approach in teaching the e hardware verification language within the context of coverage driven verification methodology I hope it will help the reader und stand the many important and interesting topics surrounding hardware verification Yoav Hollander Founder and CTO Verisity Inc Preface This book provides a detailed coverage of the e hardware verification language HVL state of the art verification methodologies and the use of e HVL as a facilitating verification tool in implementing a state of the art verification environment It includes comprehensive descriptions of the new concepts introduced by the e language e language syntax and its as ciated semantics This book also describes the architectural views and requirements of verifi tion environments randomly generated environments coverage driven verification environments etc verification blocks in the architectural views i e generators initiators c lectors checkers monitors coverage definitions etc and their implementations using the e HVL Moreover the e Reuse Methodology eRM the motivation for defining such a gui line and step by step instructions for building an eRM compliant e Verification Component eVC are also discussed   *Hardware Verification with System Verilog* Mike Mintz,Robert Ekendahl,2007-05-03 This is the second of our books designed to help the professional verifier manage complexity This time we have responded to a growing interest not only in object oriented programming but also in SystemVerilog The writing of this second handbook has been just another step in an ongoing masochistic endeavor to make your professional lives as painfree as possible The authors are not special people We have worked in several companies large and small made mistakes and generally muddled through our work There are many people in the industry who are smarter than we are and many coworkers who are more experienced However we have a strong desire to help We have been in the lab when we bring up the chips fresh from the fab with customers and sales breathing down our necks We ve been through software 1 bring up and worked on drivers that had to work around bugs in production chips What we feel makes us unique is our combined broad experience from both the software and hardware worlds Mike has over 20 years of experience from the software world that he applies in this book to hardware verification Robert has over 12 years of experience with hardware verification with a focus on environments and methodology   Verification Plans Peet James,2011-06-28 Verification isjob one in today s modem design process Statistics tell us that the verification process takes up a majority of the overall work Chips that come back dead on arrival scream that verification is at fault for not finding the mistakes How do we ensure success After an accomplishment have you ever had someone ask you Are you good or are you just lucky Many design projects depend on blind luck in hopes that the chip will work Other s just adamantly rely on their own abilities to

bring the chip to success ill either case how can we tell the difference between being good or lucky There must be a better way not to fail Failure No one likes to fail ill his book The Logic of Failure Dietrich Domer argues that failure does not just happen A series of wayward steps leads to disaster Often these wayward steps are not really logical decisive steps but more like default omissions Anti planning if you will an ad hoc approach to doing something To not plan then is to fail

    Hardware Verification Todd Jeffry Wagner,1977 Methods for detecting logical errors in computer hardware designs using symbolic manipulation instead of digital simulation are discussed A non procedural register transfer language is proposed that is suitable for describing how a digital circuit should perform This language can also be used to describe each of the components used in the design Transformations are presented which should enable the designer to either prove or disprove that the set of interconnected components correctly satisfy the specifications for the overall system The problem of detecting timing anomalies such as races hazards and oscillations is addressed Also explored are some interesting relationships between the problems of hardware verification and program verification Finally the results of using an existing proof checking program on some digital circuits are presented Although the theorem proving approach is not very efficient for simple circuits it becomes increasingly attractive as circuits become more complex This is because the theorem proving approach can use complicated component specifications without reducing them to the gate level Author   Hardware Verification with C++ Mike Mintz,Robert Ekendahl,2006-12-11 Describes a small verification library with a concentration on user adaptability such as re useable components portable Intellectual Property and co verification Takes a realistic view of reusability and distills lessons learned down to a tool box of techniques and guidelines   *Writing Testbenches using SystemVerilog* Janick Bergeron,2007-02-02 Verification is too often approached in an ad hoc fashion Visually inspecting simulation results is no longer feasible and the directed test case methodology is reaching its limit Moore s Law demands a productivity revolution in functional verification methodology Writing Testbenches Using SystemVerilog offers a clear blueprint of a verification process that aims for first time success using the SystemVerilog language From simulators to source management tools from specification to functional coverage from I s and O s to high level abstractions from interfaces to bus functional models from transactions to self checking testbenches from directed testcases to constrained random generators from behavioral models to regression suites this book covers it all Writing Testbenches Using SystemVerilog presents many of the functional verification features that were added to the Verilog language as part of SystemVerilog Interfaces virtual modports classes program blocks clocking blocks and others SystemVerilog features are introduced within a coherent verification methodology and usage model Writing Testbenches Using SystemVerilog introduces the reader to all elements of a modern scalable verification methodology It is an introduction and prelude to the verification methodology detailed in the Verification Methodology Manual for SystemVerilog It is a SystemVerilog version of the author s bestselling book Writing Testbenches Functional Verification of HDL Models   **Current Trends in Hardware Verification and**

Automated Theorem Proving Graham Birtwistle,P.A. Subrahmanyam,2012-12-06 This report describes the partially completed correctness proof of the Viper block model Viper 7 8 9 11 23 is a microprocessor designed by W J Cullyer C Pygott and J Kershaw at the Royal Signals and Radar Establishment in Malvern England henceforth RSRE for use in safety critical applications such as civil aviation and nuclear power plant control It is currently finding uses in areas such as the de ployment of weapons from tactical aircraft To support safety critical applications Viper has a particulary simple design about which it is relatively easy to reason using current techniques and models The designers who deserve much credit for the promotion of formal methods intended from the start that Viper be formally verified Their idea was to model Viper in a sequence of decreasingly abstract levels each of which concentrated on some aspect ofthe design such as the flow ofcontrol the processingofinstructions and so on That is each model would be a specification of the next less abstract model and an implementation of the previous model if any The verification effort would then be simplified by being structured according to the sequence of abstraction levels These models or levels of description were characterized by the design team The first two levels and part of the third were written by them in a logical language amenable to reasoning and proof   Computer Hardware Description Languages and their Applications D. Borrione,R. Waxman,2014-06-28 The topic areas presented within this volume focus on design environments and the applications of hardware description and modelling including simulation verification by correctness proofs synthesis and test The strong relationship between the topics of CHDL 91 and the work around the use and re standardization of the VHDL language is also explored The quality of this proceedings and its significance to the academic and professional worlds is assured by the excellent technical programme here compiled

 Generating Hardware Assertion Checkers Marc Boulé,Zeljko Zilic,2008-06-01 Assertion based design is a powerful new paradigm that is facilitating quality improvement in electronic design Assertions are statements used to describe properties of the design I e design intent that can be included to actively check correctness throughout the design cycle and even the lifecycle of the product With the appearance of two new languages PSL and SVA assertions have already started to improve verification quality and productivity This is the first book that presents an under the hood view of generating assertion checkers and as such provides a unique and consistent perspective on employing assertions in major areas such as specification verification debugging on line monitoring and design quality improvement   Introduction to Formal Hardware Verification Thomas Kropf,2013-03-09 Hardware verification is a hot topic in circuit and system design due to rising circuit complexity This advanced textbook presents an almost complete overview of techniques for hardware verification It covers all approaches used in existing tools such as binary and word level decision diagrams symbolic methods for equivalence checking and temporal logic model checking and introduces the use of higher order logic theorem proving for verifying circuit correctness It enables the reader to understand the advantages and limitations of each technique Each chapter contains an introduction and a summary as well as a section for the advanced reader Thus a broad audience is addressed

from beginners in system design to experts   **Computer Aided Verification** Aarti Gupta,Sharad Malik,2008-06-17 This book constitutes the refereed proceedings of the 20th International Conference on Computer Aided Verification CAV 2008 held in Princeton NJ USA in July 2008 The 33 revised full papers presented together with 14 tool papers and 2 invited papers and 4 invited tutorials were carefully reviewed and selected from 104 regular paper and 27 tool paper submissions The papers are organized in topical sections on concurrency memory consistency abstraction refinement hybrid systems dynamic verification modeling and specification formalisms decision procedures program verification program and shape analysis security and program analysis hardware verification model checking space efficient algorithms and model checking

Computer Hardware Description Languages and their Applications D. Agnew,L. Claesen,R. Camposano,2014-05-21 Hardware description languages HDLs have established themselves as one of the principal means of designing electronic systems The interest in and usage of HDLs continues to spread rapidly driven by the increasing complexity of systems the growth of HDL driven synthesis the research on formal design methods and many other related advances This research oriented publication aims to make a strong contribution to further developments in the field The following topics are explored in depth BDD based system design and analysis system level formal verification formal reasoning on hardware languages for protocol specification VHDL HDL based design methods high level synthesis and text graphical HDLs There are short papers covering advanced design capture and recent work in high level synthesis and formal verification In addition several invited presentations on key issues discuss and summarize recent advances in real time system design automatic verification of sequential circuits and languages for protocol specification   **Embedded Systems Handbook** Richard Zurawski,2017-12-19 Considered a standard industry resource the Embedded Systems Handbook provided researchers and technicians with the authoritative information needed to launch a wealth of diverse applications including those in automotive electronics industrial automated systems and building automation and control Now a new resource is required to report on current developments and provide a technical reference for those looking to move the field forward yet again Divided into two volumes to accommodate this growth the Embedded Systems Handbook Second Edition presents a comprehensive view on this area of computer engineering with a currently appropriate emphasis on developments in networking and applications Those experts directly involved in the creation and evolution of the ideas and technologies presented offer tutorials research surveys and technology overviews that explore cutting edge developments and deployments and identify potential trends This second self contained volume of the handbook Network Embedded Systems focuses on select application areas It covers automotive field industrial automation building automation and wireless sensor networks This volume highlights implementations in fast evolving areas which have not received proper coverage in other publications Reflecting the unique functional requirements of different application areas the contributors discuss inter node communication aspects in the context of specific applications of networked embedded systems Those looking for guidance on

preliminary design of embedded systems should consult the first volume Embedded Systems Design and Verification

Complex Digital Circuits Jean-Pierre Deschamps,Elena Valderrama,Lluís Terés,2019-03-14 This textbook is designed for a second course on digital systems focused on the design of digital circuits It was originally designed to accompany a MOOC Massive Open Online Course created at the Autonomous University of Barcelona UAB currently available on the Coursera platform Readers will learn to develop complex digital circuits starting from a functional specification will know the design alternatives that a development engineer can choose to reach the specified circuit performance and will understand which design tools are available to develop a new circuit *DIGITAL HARDWARE MODELLING USING SYSTEMVERILOG* BATRA, S.B.,2025-05-01 This book offers a practical application oriented introduction to Digital Hardware Modelling using SystemVerilog Written in a student friendly style adopting a step by step learning approach the book simplifies the nuances of language constructs and design methodologies empowering readers to design Application Specific Integrated Circuits ASICs System on Chip SoC and Central Processing Unit CPU architectures It covers a broad spectrum of topics including SystemVerilog assertions functional coverage interfaces mailboxes and various data types presented with clarity and supported by easy to follow examples Authored by an experienced professor and practitioner of ASIC SoC CPU and FPGA design this book is grounded in hands on experience and real world application The extensive coding examples demonstrate using a wide range of SystemVerilog constructs making this a valuable reference for tackling complex multi million gate ASIC design challenges It serves as a comprehensive guide for students educators and professionals who want to master the SystemVerilog language and apply it in real world VLSI design environments Overall the book helps readers understand the role of modelling in chip fabrication KEY FEATURES Covers every aspect of SystemVerilog from introducing Modelling and SystemVerilog Hardware Description Language to Modelling a Processor in SystemVerilog Includes several coding examples to help students to model different digital hardware Covers the concepts of data path and control path frequently used in processor chips Explains the concept of pipelining used in the processor TARGET AUDIENCE B Tech Electronics Electronics and Communication Engineering B Tech Computer Science and Computer Applications Front End Engineers **Advanced VLSI Design and Testability Issues** Suman Lata Tripathi,Sobhit Saxena,Sushanta Kumar Mohapatra,2020-08-19 This book facilitates the VLSI interested individuals with not only in depth knowledge but also the broad aspects of it by explaining its applications in different fields including image processing and biomedical The deep understanding of basic concepts gives you the power to develop a new application aspect which is very well taken care of in this book by using simple language in explaining the concepts In the VLSI world the importance of hardware description languages cannot be ignored as the designing of such dense and complex circuits is not possible without them Both Verilog and VHDL languages are used here for designing The current needs of high performance integrated circuits ICs including low power devices and new emerging materials which can play a very important role in achieving new functionalities are the most interesting part of the book The

testing of VLSI circuits becomes more crucial than the designing of the circuits in this nanometer technology era The role of fault simulation algorithms is very well explained and its implementation using Verilog is the key aspect of this book This book is well organized into 20 chapters Chapter 1 emphasizes on uses of FPGA on various image processing and biomedical applications Then the descriptions enlighten the basic understanding of digital design from the perspective of HDL in Chapters 2 5 The performance enhancement with alternate material or geometry for silicon based FET designs is focused in Chapters 6 and 7 Chapters 8 and 9 describe the study of bimolecular interactions with biosensing FETs Chapters 10 13 deal with advanced FET structures available in various shapes materials such as nanowire HFET and their comparison in terms of device performance metrics calculation Chapters 14 18 describe different application specific VLSI design techniques and challenges for analog and digital circuit designs Chapter 19 explains the VLSI testability issues with the description of simulation and its categorization into logic and fault simulation for test pattern generation using Verilog HDL Chapter 20 deals with a secured VLSI design with hardware obfuscation by hiding the IC s structure and function which makes it much more difficult to reverse engineer   100 Power Tips for FPGA Designers ,   *Debugging at the Electronic System Level* Frank Rogin,Rolf Drechsler,2010-06-17 Debugging becomes more and more the bottleneck to chip design productivity especially while developing modern complex integrated circuits and systems at the Electronic System Level ESL Today debugging is still an unsystematic and lengthy process Here a simple reporting of a failure is not enough anymore Rather it becomes more and more important not only to find many errors early during development but also to provide efficient methods for their isolation In Debugging at the Electronic System Level the state of the art of modeling and verification of ESL designs is reviewed There a particular focus is taken onto SystemC Then a reasoning hierarchy is introduced The hierarchy combines well known debugging techniques with whole new techniques to improve the verification efficiency at ESL The proposed systematic debugging approach is supported amongst others by static code analysis debug patterns dynamic program slicing design visualization property generation and automatic failure isolation All techniques were empirically evaluated using real world industrial designs Summarized the introduced approach enables a systematic search for errors in ESL designs Here the debugging techniques improve and accelerate error detection observation and isolation as well as design understanding   **Library of Congress Subject Headings** Library of Congress,2010   *Guide to FPGA Implementation of Arithmetic Functions* Jean-Pierre Deschamps,Gustavo D. Sutter,Enrique Cantó,2012-04-02 This book is designed both for FPGA users interested in developing new specific components generally for reducing execution times and IP core designers interested in extending their catalog of specific components The main focus is circuit synthesis and the discussion shows for example how a given algorithm executing some complex function can be translated to a synthesizable circuit description as well as which are the best choices the designer can make to reduce the circuit cost latency or power consumption This is not a book on algorithms It is a book that shows how to translate efficiently an algorithm to a circuit

using techniques such as parallelism pipeline loop unrolling and others Numerous examples of FPGA implementation are described throughout this book and the circuits are modeled in VHDL Complete and synthesizable source files are available for download

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