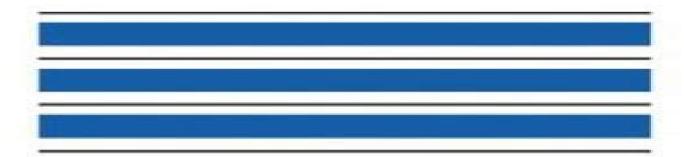# Hardware Annealing in Analog VLSI Neurocomputing

Bang W. Lee
Bing J. Sheu

Hardware Annealing In Analog Vlsi Neurocomputing

J.-P. Colinge

Hardware Annealing In Analog Vlsi Neurocomputing:

Hardware Annealing in Analog VLSI Neurocomputing Bank W. Lee,Bing J. Sheu,2012-12-06 Rapid advances in neural sciences and VLSI design technologies have provided an excellent means to boost the computational capability and efficiency of data and signal processing tasks by several orders of magnitude With massively parallel processing capabilities artificial neural networks can be used to solve many engineering and scientific problems Due to the optimized data communication structure for artificial intelligence applications a neurocomputer is considered as the most promising sixth generation computing machine Typical applica tions of artificial neural networks include associative memory pattern classification early vision processing speech recognition image data compression and intelligent robot control VLSI neural circuits play an important role in exploring and exploiting the rich properties of artificial neural networks by using pro grammable synapses and gain adjustable neurons Basic building blocks of the analog VLSI neural networks consist of operational amplifiers as electronic neurons and synthesized resistors as electronic synapses The synapse weight information can be stored in the dynamically refreshed capacitors for medium term storage or in the floating gate of an EEPROM cell for long term storage The feedback path in the amplifier can continuously change the output neuron operation from the unity gain configuration to a high gain configuration The adjustability of the vol tage gain in the output neurons allows the implementation of hardware annealing in analog VLSI neural chips to find optimal solutions very efficiently Both supervised learning and unsupervised learning can be implemented by using the programmable neural chips   **Hardware Annealing in Analog VLSI Neurocomputing** Bank W. Lee,Bing J. Sheu,2012-12-06 Rapid advances in neural sciences and VLSI design technologies have provided an excellent means to boost the computational capability and efficiency of data and signal processing tasks by several orders of magnitude With massively parallel processing capabilities artificial neural networks can be used to solve many engineering and scientific problems Due to the optimized data communication structure for artificial intelligence applications a neurocomputer is considered as the most promising sixth generation computing machine Typical applica tions of artificial neural networks include associative memory pattern classification early vision processing speech recognition image data compression and intelligent robot control VLSI neural circuits play an important role in exploring and exploiting the rich properties of artificial neural networks by using pro grammable synapses and gain adjustable neurons Basic building blocks of the analog VLSI neural networks consist of operational amplifiers as electronic neurons and synthesized resistors as electronic synapses The synapse weight information can be stored in the dynamically refreshed capacitors for medium term storage or in the floating gate of an EEPROM cell for long term storage The feedback path in the amplifier can continuously change the output neuron operation from the unity gain configuration to a high gain configuration The adjustability of the vol tage gain in the output neurons allows the implementation of hardware annealing in analog VLSI neural chips to find optimal solutions very efficiently Both supervised learning and unsupervised learning can be implemented by using the

programmable neural chips *Cellular Neural Networks and Analog VLSI* Leon Chua,Glenn Gulak,Edmund Pierzchala,Ángel Rodríguez-Vázquez,2013-03-09 Cellular Neural Networks and Analog VLSI brings together in one place important contributions and up to date research results in this fast moving area Cellular Neural Networks and Analog VLSI serves as an excellent reference providing insight into some of the most challenging research issues in the field *Symbolic Analysis for Automated Design of Analog Integrated Circuits* Georges Gielen,Willy M.C. Sansen,2012-12-06 It is a great honor to provide a few words of introduction for Dr Georges Gielen s and Prof Willy Sansen s book Symbolic analysis for automated design of analog integrated circuits The symbolic analysis method presented in this book represents a significant step forward in the area of analog circuit design As demonstrated in this book symbolic analysis opens up new possibilities for the development of computer aided design CAD tools that can analyze an analog circuit topology and automatically size the components for a given set of specifications Symbolic analysis even has the potential to improve the training of young analog circuit designers and to guide more experienced designers through second order phenomena such as distortion This book can also serve as an excellent reference for researchers in the analog circuit design area and creators of CAD tools as it provides a comprehensive overview and comparison of various approaches for analog circuit design automation and an extensive bibliography The world is essentially analog in nature hence most electronic systems involve both analog and digital circuitry As the number of transistors that can be integrated on a single integrated circuit IC substrate steadily increases over time an ever increasing number of systems will be implemented with one or a few very complex ICs because of their lower production costs *Neural Information Processing and VLSI* Bing J. Sheu,Joongho Choi,2012-12-06 Neural Information Processing and VLSI provides a unified treatment of this important subject for use in classrooms industry and research laboratories in order to develop advanced artificial and biologically inspired neural networks using compact analog and digital VLSI parallel processing techniques Neural Information Processing and VLSI systematically presents various neural network paradigms computing architectures and the associated electronic optical implementations using efficient VLSI design methodologies Conventional digital machines cannot perform computationally intensive tasks with satisfactory performance in such areas as intelligent perception including visual and auditory signal processing recognition understanding and logical reasoning where the human being and even a small living animal can do a superb job Recent research advances in artificial and biological neural networks have established an important foundation for high performance information processing with more efficient use of computing resources The secret lies in the design optimization at various levels of computing and communication of intelligent machines Each neural network system consists of massively paralleled and distributed signal processors with every processor performing very simple operations thus consuming little power Large computational capabilities of these systems in the range of some hundred giga to several tera operations per second are derived from collectively parallel processing and efficient data routing through well structured interconnection networks Deep submicron very large scale

integration VLSI technologies can integrate tens of millions of transistors in a single silicon chip for complex signal processing and information manipulation The book is suitable for those interested in efficient neurocomputing as well as those curious about neural network system applications It has beenespecially prepared for use as a text for advanced undergraduate and first year graduate students and is an excellent reference book for researchers and scientists working in the fields covered   World Congress on Neural Networks Paul Werbos,Harold Szu,Bernard Widrow,2021-09-09 Centered around 20 major topic areas of both theoretical and practical importance the World Congress on Neural Networks provides its registrants from a diverse background encompassing industry academia and government with the latest research and applications in the neural network field   *High-Level VLSI Synthesis* Raul Camposano,Wayne Wolf,2012-12-06 The time has come for high level synthesis When research into synthesizing hardware from abstract program like de scriptions started in the early 1970 s there was no automated path from the register transfer design produced by high level synthesis to a complete hardware imple mentation As a result it was very difficult to measure the effectiveness of high level synthesis methods it was also hard to justify to users the need to automate architecture design when low level design had to be completed manually Today s more mature CAD techniques help close the gap between an automat ically synthesized design and a manufacturable design Market pressures encour age designers to make use of any and all automated tools Layout synthesis logic synthesis and specialized datapath generators make it feasible to quickly imple ment a register transfer design in silicon leaving designers more time to consider architectural improvements As IC design becomes more automated customers are increasing their demands today s leading edge designers using logic synthesis systems are training themselves to be tomorrow s consumers of high level synthe sis systems The need for very fast turnaround a competitive fabrication market WhlCh makes small quantity ASIC manufacturing possible and the ever growing co n plexity of the systems being designed all make higher level design automaton inevitable   Silicon-on-Insulator Technology J.-P. Colinge,2013-03-09 5 2 Distinction between thick and thin film devices 109 5 3 I V Characteristics 112 5 3 1 Threshold voltage 11 2 5 3 2 Body effecL 1 1 8 5 3 3 Short channel effects 120 5 3 4 Output characteristics 1 24 5 4 Transconductance and mobility 129 5 4 1 Transconductance 129 5 4 2 Mobility 130 5 5 Subthreshold slope 132 5 6 Impact ionization and high field effects 13 9 5 6 1 Kink effecL 1 39 5 6 2 Hot electron degradation 143 5 7 Parasitic bipolar effects 145 5 7 1 Anomalous subthreshold slope 1 45 5 7 2 Reduced drain breakdown voltage 14 7 5 8 Accumulation mode p channel MOSFET 14 9 CHAPTER 6 Other SOl Devices 1 5 9 6 1 Non conventional devices adapted from bulk 159 6 1 1 COMFET 160 6 1 2 High voltage lateral MOSFET 1 6 1 6 1 3 PIN photodiode 162 6 1 4 JFET 163 6 2 Novel SOl devices 164 6 2 1 Lubistor 164 6 2 2 Bipolar MOS device 166 6 2 3 Double gate MOSFET 1 69 6 2 4 Bipolar transistors 172 6 2 5 Optical modulator 1 74 CHAPTER 7 The sm MOSFET Operating in a Harsh Environment 1 77 7 1 Radiation environment 1 7 7 7 1 1 SEU 178 7 1 2 Total dose 180 7 1 3 Dose rate 1 8 4 7 2 High temperature operation 1 85 7 2 1 Leakage currents   Microwave Semiconductor Devices Sigfrid

Yngvesson,2012-12-06 We have reached the double conclusion that invention is choice that this choice is imperatively governed by the sense of scientific beauty Hadamard 1945 Princeton University Press by permission The great majority of all sources and amplifiers of microwave energy and all devices for receiving or detecting microwaves use a semiconductor active element The development of microwave semiconductor devices de scribed in this book has proceeded from the simpler two terminal devices such as GUNN or IMPATT devices which originated in the 1960s to the sophisticated monolithic circuit MESFET three terminal active elements of the 1980s and 1990s The microwave field has experienced a renais sance in electrical engineering departments in the last few years and much of this growth has been associated with microwave semiconductor devices The University of Massachusetts has recently developed a well recognized program in microwave engineering Much of the momentum for this pro gram has been provided by interaction with industrial companies and the influx of a large number of industry supported students This program had a need for a course in microwave semiconductor devices which covered the physical aspects as well as the aspects of interest to the engineer who incorporates such devices in his designs It was also felt that it would be im portant to introduce the most recently developed devices HFETs HBTs and other advanced devices as early as possible   Neural Networks and Speech Processing David P. Morgan,Christopher L. Scofield,2012-12-06 We would like to take this opportunity to thank all of those individ uals who helped us assemble this text including the people of Lockheed Sanders and Nestor Inc whose encouragement and support were greatly appreciated In addition we would like to thank the members of the Lab oratory for Engineering Man Machine Systems LEMS and the Center for Neural Science at Brown University for their frequent and helpful discussions on a number of topics discussed in this text Although we both attended Brown from 1983 to 1985 and had offices in the same building it is surprising that we did not meet until 1988 We also wish to thank Kluwer Academic Publishers for their profes sionalism and patience and the reviewers for their constructive criticism Thanks to John McCarthy for performing the final proof and to John Adcock Chip Bachmann Deborah Farrow Nathan Intrator Michael Perrone Ed Real Lance Riek and Paul Zemany for their comments and assistance We would also like to thank Khrisna Nathan our most unbi ased and critical reviewer for his suggestions for improving the content and accuracy of this text A special thanks goes to Steve Hoffman who was instrumental in helping us perform the experiments described in Chapter 9   **A Survey of High-Level Synthesis Systems** Robert A. Walker,Raul Camposano,2012-12-06 After long years of work that have seen little industrial application high level synthesis is finally on the verge of becoming a practical tool The state of high level synthesis today is similar to the state of logic synthesis ten years ago At present logic synthesis tools are widely used in digital system design In the future high level synthesis will play a key role in mastering design complexity and in truly exploiting the potential of ASIes and PLDs which demand extremely short design cycles Work on high level synthesis began over twenty years ago Since substantial progress has been made in understanding the basic then problems involved although no single universally accepted theoretical framework has yet

emerged There is a growing number of publications devoted to high level synthesis specialized workshops are held regularly and tutorials on the topic are commonly held at major conferences This book gives an extensive survey of the research and development in high level synthesis In Part I a short tutorial explains the basic concepts used in high level synthesis and follows an example design throughout the synthesis process In Part II current high level synthesis systems are surveyed

Integrating Functional and Temporal Domains in Logic Design Patrick C. McGeer,Robert K. Brayton,2012-12-06 This book is an extension of one author s doctoral thesis on the false path problem The work was begun with the idea of systematizing the various solutions to the false path problem that had been proposed in the literature with a view to determining the computational expense of each versus the gain in accuracy However it became clear that some of the proposed approaches in the literature were wrong in that they under estimated the critical delay of some circuits under reasonable conditions Further some other approaches were vague and so of questionable accu racy The focus of the research therefore shifted to establishing a theory the viability theory and algorithms which could be guaranteed correct and then using this theory to justify or not existing approaches Our quest was successful enough to justify presenting the full details in a book After it was discovered that some existing approaches were wrong it became apparent that the root of the difficulties lay in the attempts to balance computational efficiency and accuracy by separating the tempo ral and logical or functional behaviour of combinational circuits This separation is the fruit of several unstated assumptions first that one can ignore the logical relationships of wires in a network when considering timing behaviour and second that one can ignore timing considerations when attempting to discover the values of wires in a circuit   Neural Models and Algorithms for Digital Testing S.T. Chadradhar,Vishwani Agrawal,M. Bushnell,2012-12-06 References 82 9 QUADRATIC 0 1 PROGRAMMING 8S 9 1 Energy Minimization 86 9 2 Notation and Tenninology 87 9 3 Minimization Technique 88 9 4 An Example 92 9 5 Accelerated Energy Minimization 94 9 5 1 Transitive Oosure 94 9 5 2 Additional Pairwise Relationships 96 9 5 3 Path Sensitization 97 9 6 Experimental Results 98 9 7 Summary 100 References 100 10 TRANSITIVE CLOSURE AND TESTING 103 10 1 Background 104 10 2 Transitive Oosure Definition 105 10 3 Implication Graphs 106 10 4 A Test Generation Algorithm 107 10 5 Identifying Necessary Assignments 112 10 5 1 Implicit Implication and Justification 113 10 5 2 Transitive Oosure Does More Than Implication and Justification 115 10 5 3 Implicit Sensitization of Dominators 116 10 5 4 Redundancy Identification 117 10 6 Summary 119 References 119 11 POLYNOMIAL TIME TESTABILITY 123 11 1 Background 124 11 1 1 Fujiwara s Result 125 11 1 2 Contribution of the Present Work 126 11 2 Notation and Tenninology 127 11 3 A Polynomial TlDle Algorithm 128 11 3 1 Primary Output Fault 129 11 3 2 Arbitrary Single Fault 135 11 3 3 Multiple Faults 137 11 4 Summary 139 References 139 ix 12 SPECIAL CASES OF HARD PROBLEMS 141 12 1 Problem Statement 142 12 2 Logic Simulation 143 12 3 Logic Circuit Modeling 146 12 3 1 Modelfor a Boolean Gate 147 12 3 2 Circuit Modeling 148 12

     Monte Carlo Device Simulation Karl Hess,2012-12-06 Monte Carlo simulation is now a well established method for

studying semiconductor devices and is particularly well suited to highlighting physical mechanisms and exploring material properties Not surprisingly the more completely the material properties are built into the simulation up to and including the use of a full band structure the more powerful is the method Indeed it is now becoming increasingly clear that phenomena such as reliabil ity related hot electron effects in MOSFETs cannot be understood satisfac torily without using full band Monte Carlo The IBM simulator DAMOCLES therefore represents a landmark of great significance DAMOCLES sums up the total of Monte Carlo device modeling experience of the past and reaches with its capabilities and opportunities into the distant future This book therefore begins with a description of the IBM simulator The second chapter gives an advanced introduction to the physical basis for Monte Carlo simulations and an outlook on why complex effects such as collisional broadening and intracollisional field effects can be important and how they can be included in the simulations References to more basic intro the book The third chapter ductory material can be found throughout describes a typical relationship of Monte Carlo simulations to experimental data and indicates a major difficulty the vast number of deformation poten tials required to simulate transport throughout the entire Brillouin zone The fourth chapter addresses possible further extensions of the Monte Carlo approach and subtleties of the electron electron interaction   *Optimal VLSI Architectural Synthesis* Catherine H. Gebotys,Mohamed I. Elmasry,2012-12-06 Although research in architectural synthesis has been conducted for over ten years it has had very little impact on industry This in our view is due to the inability of current architectural synthesizers to provide area delay competitive or optimal architectures that will support interfaces to analog asynchronous and other complex processes They also fail to incorporate testability The OASIC optimal architectural synthesis with interface constraints architectural synthesizer and the CATREE computer aided trees synthesizer demonstrate how these problems can be solved Traditionally architectural synthesis is viewed as NP hard and there fore most research has involved heuristics OASIC demonstrates by using an IP approach using polyhedral analysis that most input algo rithms can be synthesized very fast into globally optimal architectures Since a mathematical model is used complex interface constraints can easily be incorporated and solved Research in test incorporation has in general been separate from syn thesis research This is due to the fact that traditional test research has been at the gate or lower level of design representation Nevertheless as technologies scale down and complexity of design scales up the push for reducing testing times is increased On way to deal with this is to incorporate test strategies early in the design process The second half of this text examines an approach for integrating architectural synthesis with test incorporation Research showed that test must be considered during synthesis to provide good architectural solutions which minimize Xlll area delay cost functions   Fault Covering Problems in Reconfigurable VLSI Systems Ran Libeskind-Hadas,Nany Hasan,Jingsheng Jason Cong,Philip McKinley,C.L. Liu,2012-12-06 Fault Covering Problems in Reconfigurable VLSI Systems describes the authors recent research on reconfiguration problems for fault tolerance in VLSI and WSI Systems The book examines solutions to a number of reconfiguration problems Efficient

algorithms are given for tractable covering problems and general techniques are given for dealing with a large number of intractable covering problems The book begins with an investigation of algorithms for the reconfiguration of large redundant memories Next a number of more general covering problems are considered and the complexity of these problems is analyzed Finally a general and uniform approach is proposed for solving a wide class of covering problems The results and techniques described here will be useful to researchers and students working in this area As such the book serves as an excellent reference and may be used as the text for an advanced course on the topic **The Industrial Electronics Handbook** J. David Irwin,1997-05-09 From traditional topics that form the core of industrial electronics to new and emerging concepts and technologies The Industrial Electronics Handbook in a single volume has the field covered Nowhere else will you find so much information on so many major topics in the field For facts you need every day and for discussions on topics you have only dreamed of The Industrial Electronics Handbook is an ideal reference *The Design of Communicating Systems* C.J. Koomen,2012-12-06 The professional schools will resume their professional responsibilities just to the degree that they can discover a science of design a body of intellectually tough partly formalizable partly empirical teachable doctrine about the design process H A Simon 1968 Design is aimed at the transformation or translation of a specification or high level description into a description in terms of some real world primitives As such it involves the removal of the uncertainty about the way in which a required system can be realized To optimally support the design of systems we must look at the design process as a whole and at the strong relationship that exists between a designer the applied design method the required design tools and the ways in which designs can be expressed This book focuses on that relationship The application field we are concerned with is the design of systems in which the communication between system elements is a major design feature Examples of such communicating systems are communication protocols telephone exchange control systems process control systems highly modular systems embedded software interactive systems and VLSI systems In summary we are concerned with systems in which concurrency plays a major role concurrency defines the mutual relationship between the activities in the different parts of a system or within a collection of systems *Parallel Algorithms and Architectures for DSP Applications* Magdy A. Bayoumi,2012-12-06 Over the past few years the demand for high speed Digital Signal Proces sing DSP has increased dramatically New applications in real time image processing satellite communications radar signal processing pattern recogni tion and real time signal detection and estimation require major improvements at several levels algorithmic architectural and implementation These perfor mance requirements can be achieved by employing parallel processing at all levels Very Large Scale Integration VLSI technology supports and provides a good avenue for parallelism Parallelism offers efficient sohitions to several problems which can arise in VLSI DSP architectures such as 1 Intermediate data communication and routing several DSP algorithms such as FFT involve excessive data routing and reordering Parallelism is an efficient mechanism to minimize the silicon cost and speed up the pro cessing

time of the intermediate middle stages 2 Complex DSP applications the required computation is almost doubled Parallelism will allow two similar channels processing at the same time The communication between the two channels has to be minimized 3 Applicatilm specific systems this emerging approach should achieve real time performance in a cost effective way 4 Testability and fault tolerance reliability has become a required feature in most of DSP systems To achieve such property the involved time overhead is significant Parallelism may be the solution to maintain ac ceptable speed performance

Digital Speech Processing A. Nejat Ince,2013-03-09 After alm ost three scores of years of basic and applied research the field of speech processing is at present undergoing a rapid growth in terms of both performance and applications and this is fueHed by the advances being made in the areas of microelectronics computation and algorithm design Speech processing relates to three aspects of voice communications Speech Coding and transmission which is mainly concerned with man to man voice communication Speech Synthesis which deals with machine to man communication Speech Recognition which is related to man to machine communication Widespread application and use of low bit rate voice codec synthesizers and recognizers which are all speech processing products requires ideaHy internationally accepted quality assessment and evaluation methods as weH as speech processing standards so that they may be interconnected and used independently of their designers and manufacturers without costly interfaces This book presents in a tutorial manner both fundamental and applied aspects of the above topics which have been prepared by weH known specialists in their respective areas The book is based on lectures which were sponsored by AGARD NATO and delivered by the authors in several NATO countries to audiences consisting mainly of academic and industrial R D engineers and physicists as weH as civil and military C3I systems planners and designers

Reviewing **Hardware Annealing In Analog Vlsi Neurocomputing**: Unlocking the Spellbinding Force of Linguistics

In a fast-paced world fueled by information and interconnectivity, the spellbinding force of linguistics has acquired newfound prominence. Its capacity to evoke emotions, stimulate contemplation, and stimulate metamorphosis is really astonishing. Within the pages of "**Hardware Annealing In Analog Vlsi Neurocomputing**," an enthralling opus penned by a highly acclaimed wordsmith, readers attempt an immersive expedition to unravel the intricate significance of language and its indelible imprint on our lives. Throughout this assessment, we shall delve in to the book is central motifs, appraise its distinctive narrative style, and gauge its overarching influence on the minds of its readers.

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Hardware Annealing In Analog Vlsi Neurocomputing Introduction

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