

# Fundamentals of Logic Design

Dr. Kiran Bailey

## Procedural Blocks

### **always and initial**

Most of the programming languages (e.g. C, Basic) are **sequential** in nature, or only one active process at any one time. However, hardware circuitry is **concurrent** in nature. All the circuitries are active in parallel.

Verilog supports parallelism by allowing any number of “**always**” and “**initial**” blocks. Each “**always**” and “**initial**” block run **concurrently**.

“**always**” and “**initial**” blocks are called **procedural blocks**. Assignment inside procedural blocks are called **procedural assignment**.

### **always and initial (cont)**

Features procedural assignment

# Fundamentals Of Logic Design West Series In Electrical Engineering

**Jorge L. Diaz-Herrera**



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