

FROM

ASICs TO SOCs

A Practical Approach



Farzad Nekoogar
Faranak Nekoogar

From Asics To Socs A Practical Approach

Dennis Derickson, Marcus Müller



From Asics To Socs A Practical Approach:

From ASICs to SOCs Farzad Nekoogar, Faranak Nekoogar, 2003 From ASICs to SOCs A Practical Approach by Farzad Nekoogar and Faranak Nekoogar covers the techniques principles and everyday realities of designing ASICs and SOCs Material includes current issues in the field front end and back end designs integration of IPs on SOC designs and low power design techniques and methodologies Appropriate for practicing chip designers as well as graduate students in electrical engineering *From Asics To Socs, 1/e* Faranak Nekoogar, 2003 *Heterogeneous SoC Design and Verification* Khaled Salah Mohamed, 2024-03-22 This book covers the foundations of hardware software codesign on chip communication debugging and verification for heterogenous SoCs Its primary objective is to empower designers in making informed decisions guiding them to strike the perfect balance between flexibility and performance for their SoC designs Readers will benefit from a detailed exploration of the essential elements of the hardware and software codesign framework accompanied by a discussion of the driving motivations behind this approach The author also provides an in depth review of various hardware design architectures shedding light on different design possibilities Furthermore the book presents key concepts concerning hardware and software communication unraveling the intricate interactions within an SoC This book provides a holistic introduction to the methodologies underpinning SoC design and verification making it an indispensable companion for both novice and experienced designers navigating the ever evolving landscape of hardware software codesign **Design**

Verification with E Samir Palnitkar, 2004 As part of the Modern Semiconductor Design series this book details a broad range of e based topics including modelling constraint driven test generation functional coverage and assertion checking

Printed Circuit Board Designer's Reference Christopher T. Robertson, 2004 PCB design instruction and reference manual all in one book with in depth explanation of the processes and tools used in modern PCB design Standards formulas definitions and procedures plus software to tie it all together [Engineering the Complex SOC](#) Chris Rowen, 2008-11-11 [Engineering the Complex SOC](#) The first unified hardware software guide to processor centric SOC design Processor centric approaches enable SOC designers to complete far larger projects in far less time [Engineering the Complex SOC](#) is a comprehensive example driven guide to creating designs with configurable extensible processors Drawing upon Tensilica s Xtensa architecture and TIE language Dr Chris Rowen systematically illuminates the issues opportunities and challenges of processor centric design Rowen introduces a radically new design methodology then covers its essential techniques processor configuration extension hardware software co generation multiple processor partitioning communication and more Coverage includes Why extensible processors are necessary shortcomings of current design methods Comparing extensible processors to traditional processors and hardwired logic Extensible processor architecture and mechanisms of processor extensibility Latency throughput coordination of parallel functions hardware interconnect options management of design complexity and other issues Multiple processor SOC architecture for embedded systems Task design from the viewpoints of

software and hardware developers Advanced techniques implementing complex state machines task to task synchronization power optimization and more Toward a sea of processors Long term trends in SOC design and semiconductor technology For all architects hardware engineers software designers and SOC program managers involved with complex SOC design and for all managers investing in SOC designs platforms processors or expertise PRENTICE HALL Professional Technical Reference Upper Saddle River NJ 07458 www.phptr.com

Metamodeling-driven IP Reuse for SoC Integration and Microprocessor Design Deepak A. Mathaikutty, Sandeep Shukla, 2009 This cutting edge resource offers you an in depth understanding of metamodeling approaches for the reuse of intellectual properties IPs in the form of reusable design or verification components The book covers the essential issues associated with fast and effective integration of reusable design components into a system on a chip SoC to achieve faster design turn around time Moreover it addresses key factors related to the use of reusable verification IPs for a write once use many times verification strategy another effective approach that can attain a faster product design cycle

Mobile, Secure, and Programmable Networking Éric Renault, Selma Boumerdassi, Cherkaoui Leghris, Samia Bouzefrane, 2019-06-20 This book constitutes the thoroughly refereed post conference proceedings of the 5th International Conference on Mobile Secure and Programmable Networking held in Mohammedia Morocco in April 2019 The 23 papers presented in this volume were carefully reviewed and selected from 48 submissions They discuss new trends in networking infrastructures security services and applications while focusing on virtualization and cloud computing for networks network programming software defined networks SDN and their security

Timing Analysis and Simulation for Signal Integrity Engineers Greg Edlund, 2007-10-22 Every day companies call upon their signal integrity engineers to make difficult decisions about design constraints and timing margins Can I move these wires closer together How many holes can I drill in this net How far apart can I place these chips Each design is unique there s no single recipe that answers all the questions Today s designs require ever greater precision but design guides for specific digital interfaces are by nature conservative Now for the first time there s a complete guide to timing analysis and simulation that will help you manage the tradeoffs between signal integrity performance and cost Writing from the perspective of a practicing SI engineer and team lead Greg Edlund of IBM presents deep knowledge and quantitative techniques for making better decisions about digital interface design Edlund shares his insights into how and why digital interfaces fail revealing how fundamental sources of pathological effects can combine to create fault conditions You won t just learn Edlund s expert techniques for avoiding failures you ll learn how to develop the right approach for your own projects and environment Coverage includes Systematically ensure that interfaces will operate with positive timing margin over the product s lifetime without incurring excess cost Understand essential chip to chip timing concepts in the context of signal integrity Collect the right information upfront so you can analyze new designs more effectively Review the circuits that store information in CMOS state machines and how they fail Learn how to time common clock source synchronous and high speed serial transfers

Thoroughly understand how interconnect electrical characteristics affect timing propagation delay impedance profile crosstalk resonances and frequency dependent loss Model 3D discontinuities using electromagnetic field solvers Walk through four case studies coupled differential vias land grid array connector DDR2 memory data transfer and PCI Express channel Appendices present a refresher on SPICE modeling and a high level conceptual framework for electromagnetic field behavior Objective realistic and practical this is the signal integrity resource engineers have been searching for Preface xiii Acknowledgments xvi About the Author xix About the Cover xx Chapter 1 Engineering Reliable Digital Interfaces 1 Chapter 2 Chip to Chip Timing 13 Chapter 3 Inside IO Circuits 39 Chapter 4 Modeling 3D Discontinuities 73 Chapter 5 Practical 3D Examples 101 Chapter 6 DDR2 Case Study 133 Chapter 7 PCI Express Case Study 175 Appendix A A Short CMOS and SPICE Primer 209 Appendix B A Stroll Through 3D Fields 219 Endnotes 233 Index 235

Signal and Power Integrity--simplified
Eric Bogatin,2010 With the inclusion of the two new hot topics in signal integrity power integrity and high speed serial links this book will be the most up to date complete guide to understanding and designing for signal integrity

Modern VLSI Design Wayne Wolf,2008-12-21 The Number 1 VLSI Design Guide Now Fully Updated for IP Based Design and the Newest Technologies Modern VLSI Design Fourth Edition offers authoritative up to the minute guidance for the entire VLSI design process from architecture and logic design through layout and packaging Wayne Wolf has systematically updated his award winning book for today s newest technologies and highest value design techniques Wolf introduces powerful new IP based design techniques at all three levels gates subsystems and architecture He presents deeper coverage of logic design fundamentals clocking and timing and much more No other VLSI guide presents as much up to date information for maximizing performance minimizing power utilization and achieving rapid design turnarounds

Digital Communications Test and Measurement Dennis Derickson,Marcus Müller,2007-12-10 A Comprehensive Guide to Physical Layer Test and Measurement of Digital Communication Links Today s new data communication and computer interconnection systems run at unprecedented speeds presenting new challenges not only in the design but also in troubleshooting test and measurement This book assembles contributions from practitioners at top test and measurement companies component manufacturers and universities It brings together information that has never been broadly accessible before information that was previously buried in application notes seminar and conference presentations short courses and unpublished works Readers will gain a thorough understanding of the inner workings of digital high speed systems and learn how the different aspects of such systems can be tested The editors and contributors cover key areas in test and measurement of transmitters digital waveform and jitter analysis and bit error ratio receivers sensitivity jitter tolerance and PLL CDR characterization and high speed channel characterization in time and frequency domain Extensive illustrations are provided throughout Coverage includes Signal integrity from a measurement point of view Digital waveform analysis using high bandwidth real time and sampling equivalent time oscilloscopes Bit error ratio measurements for both electrical and optical links Extensive coverage on the

topic of jitter in high speed networks State of the art optical sampling techniques for analysis of 100 Gbit s signals Receiver characterization clock recovery phase locked loops jitter tolerance and transfer functions sensitivity testing and stressed waveform receiver testing Channel and system characterization TDR T and frequency domain based alternatives Testing and measuring PC architecture communication links PCIexpress SATA and FB DIMM Jitter, Noise, and Signal Integrity at High-Speed Mike Peng Li,2007-11-19 State of the art JNB and SI Problem Solving Theory Analysis Methods and Applications Jitter noise and bit error JNB and signal integrity SI have become today s greatest challenges in high speed digital design Now there s a comprehensive and up to date guide to overcoming these challenges direct from Dr Mike Peng Li cochair of the PCI Express jitter standard committee One of the field s most respected experts Li has brought together the latest theory analysis methods and practical applications demonstrating how to solve difficult JNB and SI problems in both link components and complete systems Li introduces the fundamental terminology definitions and concepts associated with JNB and SI as well as their sources and root causes He guides readers from basic math statistics circuit and system models all the way through final applications Emphasizing clock and serial data communications applications he covers JNB and SI simulation modeling diagnostics debugging compliance testing and much more **Power Integrity Modeling and Design for Semiconductors and Systems** Madhavan Swaminathan,Ege Engin,2007-11-19 The First Comprehensive Example Rich Guide to Power Integrity Modeling Professionals such as signal integrity engineers package designers and system architects need to thoroughly understand signal and power integrity issues in order to successfully design packages and boards for high speed systems Now for the first time there s a complete guide to power integrity modeling everything you need to know from the basics through the state of the art Using realistic case studies and downloadable software examples two leading experts demonstrate today s best techniques for designing and modeling interconnects to efficiently distribute power and minimize noise The authors carefully introduce the core concepts of power distribution design systematically present and compare leading techniques for modeling noise and link these techniques to specific applications Their many examples range from the simplest using analytical equations to compute power supply noise through complex system level applications The authors Introduce power delivery network components analysis high frequency measurement and modeling requirements Thoroughly explain modeling of power ground planes including plane behavior lumped modeling distributed circuit based approaches and much more Offer in depth coverage of simultaneous switching noise including modeling for return currents using time and frequency domain analysis Introduce several leading time domain simulation methods such as macromodeling and discuss their advantages and disadvantages Present the application of the modeling methods on several advanced case studies that include high speed servers high speed differential signaling chip package analysis materials characterization embedded decoupling capacitors and electromagnetic bandgap structures This book s system level focus and practical examples will make it indispensable for every student and professional concerned with power integrity including electrical

engineers system designers signal integrity engineers and materials scientists It will also be valuable to developers building software that helps to analyze high speed systems

Real World FPGA Design with Verilog Ken Coffman, 1999-12-08 The practical guide for every circuit designer creating FPGA designs with Verilog Walk through design step by step from coding through silicon Partitioning synthesis simulation test benches combinatorial and sequential designs and more Real World FPGA Design with Verilog guides you through every key challenge associated with designing FPGAs and ASICs using Verilog one of the world's leading hardware design languages You'll find irreverent yet rigorous coverage of what it really takes to translate HDL code into hardware and how to avoid the pitfalls that can occur along the way Ken Coffman presents no frills real world design techniques that can improve the stability and reliability of virtually any design Start by walking a typical Verilog design all the way through to silicon then review basic Verilog syntax design simulation and testing advanced simulation and more Coverage includes Essential digital design strategies recognizing the underlying analog building blocks used to create digital primitives implementing logic with LUTs clocking strategies logic minimization and more Key engineering tradeoffs including operating speed vs latency Combinatorial and sequential designs Verilog test fixtures compiler directives and automated testing A detailed comparison of alternative architectures and software including a never before published FPGA technology selection checklist Real World FPGA Design with Verilog introduces libraries and reusable modules points out opportunities to reuse your own code and helps you decide when to purchase existing IP designs instead of building from scratch Essential rules for designing with ASIC conversion in mind are presented If you're involved with digital hardware design with Verilog Ken Coffman is a welcome voice of experience showing you the shortcuts helping you over the rough spots and helping you achieve competence faster than you ever expected

A Signal Integrity Engineer's Companion Geoff Lawday, David Ireland, Greg Edlund, 2008-06-12 A Signal Integrity Engineer's Companion Real Time Test and Measurement and Design Simulation Geoff Lawday David Ireland Greg Edlund Foreword by Chris Edwards Editor IET Electronics Systems and Software magazine Prentice Hall Modern Semiconductor Design Series Prentice Hall Signal Integrity Library Use Real World Test and Measurement Techniques to Systematically Eliminate Signal Integrity Problems This is the industry's most comprehensive authoritative and practical guide to modern Signal Integrity SI test and measurement for high speed digital designs Three of the field's leading experts guide you through systematically detecting observing analyzing and rectifying both modern logic signal defects and embedded system malfunctions The authors cover the entire life cycle of embedded system design from specification and simulation onward illuminating key techniques and concepts with easy to understand illustrations Writing for all electrical engineers signal integrity engineers and chip designers the authors show how to use real time test and measurement to address today's increasingly difficult interoperability and compliance requirements They also present detailed start to finish case studies that walk you through commonly encountered design challenges including ensuring that interfaces consistently operate with positive timing

margins without incurring excessive cost calculating total jitter budgets and managing complex tradeoffs in high speed serial interface design Coverage includes Understanding the complex signal integrity issues that arise in today s high speed designs Learning how eye diagrams automated compliance tests and signal analysis measurements can help you identify and solve SI problems Reviewing the electrical characteristics of today s most widely used CMOS IO circuits Performing signal path analyses based on intuitive Time Domain Reflectometry TDR techniques Achieving more accurate real time signal measurements and avoiding probe problems and artifacts Utilizing digital oscilloscopes and logic analyzers to make accurate measurements in high frequency environments Simulating real world signals that stress digital circuits and expose SI faults Accurately measuring jitter and other RF parameters in wireless applications About the Authors Dr Geoff Lawday is Tektronix Professor in Measurement at Buckinghamshire New University England He delivers courses in signal integrity engineering and high performance bus systems at the University Tektronix laboratory and presents signal integrity seminars throughout Europe on behalf of Tektronix David Ireland European and Asian design and manufacturing marketing manager for Tektronix has more than 30 years of experience in test and measurement He writes regularly on signal integrity for leading technical journals Greg Edlund Senior Engineer IBM Global Engineering Solutions division has participated in development and testing for ten high performance computing platforms He authored Timing Analysis and Simulation for Signal Integrity Engineers Prentice Hall Signal Integrity Issues and Printed Circuit Board Design Douglas Brooks,2003 Complicated concepts explained succinctly and in laymen s terms to both experienced and novice PCB designers Numerous examples allow reader to visualize how high end software simulators see various types of SI problems and then their solutions Author is a frequent and recognized seminar leader in the industry *Signal Integrity* Eric Bogatin,2004 This thorough review of the fundamental principles associated with signal integrity provides engineering principles behind signal integrity effects and applies this understanding to solving problems **Essential Electronic Design Automation (EDA)** Mark Birnbaum,2004 Describes the engineering needs addressed by the individual EDA tools and covers EDA from both the provider and user viewpoints Learn the importance of marketing and business trends in the EDA industry The EDA consortium is made up of major corporations including SUN HP and Intel **Software Engineering 3** Dines Bjørner,2006-03-09 The final installment in this three volume set is based on this maxim Before software can be designed its requirements must be well understood and before the requirements can be expressed properly the domain of the application must be well understood The book covers the process from the development of domain descriptions through the derivation of requirements prescriptions from domain models to the refinement of requirements into software architectures and component design

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